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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

Sheet 1

of 2

Complete if Known

Application Number	101630,615
Filing Date	07/30/2003
First Named Inventor	Josey G. Angilivelil
Art Unit	2825
Examiner Name	NGHIA M. DEAT
Attorney Docket Number	TI-34945

U. S. PATENT DOCUMENTS

FOREIGN PATENT DOCUMENTS

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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Sheet

2

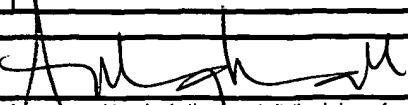
of

2

Complete If Known	
Application Number	101630,615
Filing Date	07/30/2003
First Name Inventor	Josey G. Angilivelil
Art Unit	2826
Examiner Name	NGUYEN M. DOAN
Attorney Docket Number	TI-34945

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
NMD		SAMY R. MAKAR and EDWARD J. MCCLUSKEY, "Iddq Test Pattern Generation for Scan Chain Latches and Flip-Flops", Center for Reliable Computing Standford University, (date unknown)	
NMD		SAGAR SBADE and DUNCAN M. WALKER, "Iddq Test: Will It Survive the DSM Challenge", Department of Computer Science Texas A&M Univiersity, pp. 1-18, (date Unknown)	
NMD		KRISTIAN WIKLUND, TOMAS MAGNUSSON and PETER DAHLGREN, "Switch-Level Fault Simulation and Test Generation For Competing Bridging Faults", Department of Computer Engineering, Chalmers University of Technology, (date unknown)	
NMP		PETER C. MAXWELL and ROBERT C. AITKEN, "Test Sets and Reject Rates: All Fault Coverages Are Not Created Equal", IEEE Design & Test of Computers, pp. 42-51, March 1993	
NWD		SHARAD C. SETH and VISHWANI D. AGRAWAL, "Characterizing the LSI Yield Equation from Wafer Test Data", IEEE Transactions on Computer-Aided Design, Vol. CAD-3, No. 2, pp. 123-126, April 1984	

Examiner Signature		Date Considered	11/28/03
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